In the Abstract

A NAND flash memory cell row ~~and the manufacturing method thereof are provided. The memory cell row~~ includes first and second stacked gate structures, control and floating gates, ~~an~~ intergate dielectric layer, a tunnel oxide layer, doping regions and source/drain regions. ~~Each of t~~The first stacked gate structures has an erase gate dielectric layer, an erase gate and a first cap layer. ~~Each of t~~The second stacked gate structure has a select gate dielectric layer, a select gate and a second cap layer. The control gate is ~~disposed~~ between each of the first stacked gate structures, and between each of the second stacked gate structures and ~~the~~ adjacent first stacked gate structure. The floating gate is ~~disposed~~ between the control gate and ~~the~~ substrate ~~and has a concave surface with a sharp edge~~. The inter-gate dielectric layer is ~~disposed~~ between the control and floating gates. The tunnel oxide is ~~disposed~~ between the floating gate and ~~the~~ substrate. ~~Furthermore,~~ tThe doping regions are ~~disposed~~ under the first stacked gate structure, and the source/drain regions are ~~disposed~~ in the exposed substrate ~~at the outer side of the second stacked gate structure~~.